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S1    4647579   ENTRY? OR NODE? OR OBJECT? OR ENTRIES OR CHILD? OR PARENT?
            OR BRANCH?
S2    8318522   ATTRIBUTE? OR NAME? OR TIMESTAMP? OR FIELD? OR CHARACTERIS-
            TIC?
S3    2004193   ERROR? OR INCORRECT? OR UNACCEPTABL? OR VERIF? OR WRONG? OR
             INVALID?
S4    4963738   MESSAG? OR ALERT? OR WARN? OR CONDITION? OR FLAG OR FLAGS
S5     613478   TREE OR TREES OR DIRECTORY OR DIRECTORIES OR BTREE OR RTREE
            OR TRIE OR TRIES OR DATA()(STRUCTURE?) OR DATASTRUCTURE?
S6    2518612   INSERT? OR ADD OR ADDS OR ADDED OR EMBED OR ADDING OR EMBE-
            DING OR INTRODUCE? OR INTRODUCING
S7         46   S1 AND S2 AND S3 AND S4 AND S5 AND S6
S8        251   S1 AND S2 AND S3 AND S5 AND S6
S9        139   S2 AND S3 AND S4 AND S5 AND S6
S10     16443   S6(2N)S1
S11        14   S10 AND (S8 OR S9)
S12     10669   S1(2N)S3
S13         4   (S8 OR S9) AND S12
S14        60   S13 OR S7 OR S11
S15        49   RD (unique items)
S16        41   S15 NOT PY>2001
File   8:Ei Compendex(R) 1970-2005/May W3
         (c) 2005 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2005/May
         (c) 2005 ProQuest Info&Learning
File  65:Inside Conferences 1993-2005/May W5
         (c) 2005 BLDSC all rts. reserv.
File   2:INSPEC 1969-2005/May W4
         (c) 2005 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2005/Apr W2
         (c)2005 Japan Science and Tech Corp(JST)
File 111:TGG Natl.Newspaper Index(SM) 1979-2005/Jun 01
         (c) 2005 The Gale Group
File   6:NTIS 1964-2005/May W4
         (c) 2005 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2005/May W4
         (c) 2005 INIST/CNRS
File  34:SciSearch(R) Cited Ref Sci 1990-2005/May W5
         (c) 2005 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2005/Apr
         (c) 2005 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2005/Apr W4
         (c) 2005 FIZ TECHNIK
```

16/5/6 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03629813 E.I. No: EIP93050797997
Title: TREE **-EXPERT: A** tree **-based expert system for fault** tree **construction**
Author: Xie, Gang; Xue, Dazhi; Xi, Shuren
Corporate Source: Tsinghua Univ, Beijing, China
Source: Reliability Engineering & System Safety v 40 n 3 1993. p 295-309
Publication Year: 1993
CODEN: RESSEP ISSN: 0951-8320
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); T; (Theoretical)
Journal Announcement: 9307W1
Abstract: This paper addresses the topic of automatic fault **tree** construction, utilizing an expert system with Artificial Intelligence (AI) techniques and presents the related software tool, **TREE** -EXPERT - an expert system for automatic fault **tree** construction. In the light of the features involved in developing a fault **tree** , a new and more reasonable structure of knowledge representation, which is knowledge **tree** based, has been established. The knowledge **tree** provides the means by which component failure behaviors can be described by a group of particular fault **tree** modules instead of production rules. By **introducing** the **conditional branch** function, the new design of the knowledge base incorporates many good features such as strong expressivity, flexibility and ease of extension and it takes advantage of the user's familiarity with the **field** of fault **tree** analysis. Additionally, the design of the inference engine is original in that it deals with **nodes** , which it treats, as special components, so that many complicated engineering cases, such as the application of success criteria, and the problems of flow diversions and flow reversals in a process system, can be well managed and the function of the expert system is improved as a whole. **TREE** -EXPERT can be used to deal with large-scale and complicated engineering systems, and many engineering factors can be considered, e.g. more than one system parameter and the effect on them switching of the system operating states, bi-directional inference, human **error** failure, common-cause failure, maintenance and test, etc. On the other hand, the software uses P & ID (Pipe & Instrument Diagram) type interface to describe the system topology, which provides an easier man-machine interface with powerful graphics functions. This software can handle not only ?process' systems but also, with appropriate additions to the generic knowledge base, electrical systems and other similar systems. (Author abstract) 12 Refs.
Descriptors: *Expert systems; **Trees** (mathematics); Failure analysis; Automation; Computer software; Topology; Interfaces (computer); Man machine systems; Computer simulation; Artificial intelligence
Identifiers: Software tool **TREE** EXPERT; Probability safety analysis (PSA)
Classification Codes:
723.4.1 (Expert Systems)
723.4 (Artificial Intelligence); 914.1 (Accidents & Accident Prevention); 731.2 (Control System Applications); 723.1 (Computer Programming); 912.2 (Management)
723 (Computer Software); 921 (Applied Mathematics); 914 (Safety Engineering); 731 (Automatic Control Principles); 912 (Industrial Engineering & Management)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS); 91 (ENGINEERING MANAGEMENT); 73 (CONTROL ENGINEERING)

16/5/14 (Item 5 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01540741 ORDER NO: AAD97-12820
THREE DIMENSIONAL ADAPTIVE FINITE ELEMENT COMPUTATION FOR ELECTROMAGNETIC FIELD PROBLEMS (MESH REFINEMENT, ERROR **ESTIMATION)**

Author: CHELLAMUTHU, K. C.
Degree: PH.D.
Year: 1996
Corporate Source/Institution: THE UNIVERSITY OF AKRON (0003)
Adviser: NATHAN IDA
Source: VOLUME 57/11-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 7118. 254 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0544

Numerical modeling involving Finite Element method provides solutions with an accuracy of 5 to 10% **error** which is acceptable for most applications. But for certain applications, higher solution accuracy is required. Since the solution accuracy depends on the spatial decomposition of a problem domain, selective discretization using adaptive finite element mesh refinement is necessary. When the problem solution is plagued by the presence of domain singularities such as boundary layers, re-entrant corners, sharp bends, cracks or multiple material discontinuities, it is necessary to selectively **add** more degrees of freedom where the solution varies abruptly.

In this dissertation a new technique is proposed for the adaptive mesh refinement and 'a posteriori' **error** estimation. A minimal hierarchical **tree** based mesh refinement algorithm and a dynamic **tree data structure** are designed and implemented to solve 2D and 3D boundary value problems in electromagnetics. The adaptive mesh utilizes first order isoparametric quadrilateral elements in 2D and isoparametric hexahedral brick elements in 3D. The mesh refinement algorithm is based on a one-level rule and refine the larger neighbor first approach. The one-level rule enables a gradual transition of a mesh providing a smooth solution near the vicinity of singular regions. In this approach, the number of **tree** traversal normally required to locate an element for refinement is minimized by utilizing the minimal **tree** and the natural sequence of element numbers. The minimization of **tree** traversal is a specific feature of the proposed algorithm compared to other techniques reported in the literature.

The generation of an optimal adaptive mesh depends on the availability of an efficient and reliable 'a posteriori' **error** estimate. Four different 'a posteriori' **error** estimation techniques are proposed in this dissertation. The first one is a post-processing and interpolation procedure which is based on the post-processed solution and the solution interpolated on a refined mesh. The second method is formulated by computing the **error** in the gradient of the **field** . In the third approach a local **error** problem is formulated on a patch of elements connected to a **node** and the local problem is solved by using the h-p, version of adaptive mesh refinement. In the fourth method an 'a posteriori' **error** is computed using the reduced continuity **condition** of edge elements and the local **field** approximation using magnetic vector potential A. The reliability assessment of two different **error** estimates viz., post-processing and gradient of **field** method through asymptotic exactness is established using the global effectivity index. The gradient of **field** method and the local **error** estimation techniques are **verified** to be simple and less expensive to implement.

The proposed mesh refinement algorithm and the **error** estimation strategies were tested by solving many 2D and 3D boundary value problems in electromagnetics. The sequence of adaptive meshes and the numerical test results establish the application potential of the proposed mesh refinement algorithm and **error** estimation techniques to model large scale problems with or without singularities.

16/5/17 (Item 8 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01323885 ORDER NO: AAD93-32526
HIGH SPEED COMMUNICATION SUPPORT FOR MULTIMEDIA APPLICATIONS: TREE NETWORK AND RECONFIGURABLE TRANSPORT PROTOCOL (NETWORK ARCHITECTURES)

Author: HUANG, HUNG KHEI
Degree: PH.D.
Year: 1993
Corporate Source/Institution: UNIVERSITY OF CALIFORNIA, IRVINE (0030)
Chair: TATSUYA SUDA
Source: VOLUME 54/07-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 3707. 197 PAGES
Descriptors: COMPUTER SCIENCE
Descriptor Codes: 0984

The development of high-speed network is essential to adequately support an increasingly diverse distributed multimedia applications that are available. Many of those applications have communication requirements that extend beyond those found in traditional data applications. Both the underlying network and transport protocol infrastructure are very important factors that significantly affect the performance of high-speed networks. The underlying network infrastructure implements the lower-layer, link-to-link protocols primarily in hardware. The transport protocol infrastructure integrates higher-layer, end-to-end network protocols. In this dissertation, we address issues on both network and transport protocol infrastructures.

First, as an underlying network infrastructure, we propose a new high speed network architecture called Collision Avoidance Multiple Broadcast (CAMB) **Tree** network. The network consists of collision avoidance switches organized in a **tree** topology. Each switch is an internal **node** in the **tree** . Stations are the leaves of the **tree** . The switches allow the implementation of random access protocols (simple and easy implementation) without its major disadvantage: the penalty of collisions among packets. **Tree** network solves the problem of packet collisions without incurring overheads (e.g., access coordination) **introduced** by controlled access protocols (e.g., FDDI, and DQDB). It combines the benefits of random access (low delay when traffic is light; simple, distributed, and robust protocols) with concurrency of transmission, excellent network utilization and suitability for the domain of high-speed optical networking. A design and implementation of the **Tree** network is presented. Performance results are obtained from the network prototype implemented, validating the concepts of the CAMB **Tree** Network. We also build a simulation model, based on the prototype. We compared the performance of the **Tree** Network with other network architectures (Ethernet, Token-Ring, FDDI), showing better performance results for the **Tree** Network. Simulations of large networks are also presented.

Second, in the transport protocol infrastructure area, we propose a transport protocol reconfiguration scheme. Reconfiguration provides adaptivity to transport protocol, enabling it to adjust to the highly diverse and dynamic applications and network **characteristics** . We designed and implemented the reconfiguration scheme for one of the major transport protocol functions: **error** handling. Three **error** handling mechanisms are considered: (1) cumulative acknowledgement with go-back-n, (2) selective acknowledgment with selective repeat and (3) forward **error** correction. We empirically evaluate these mechanisms using several different applications (such as data, voice and video) that run in a simulated network environment. Through these experiments we determine (1) efficient combinations of application/mechanism/network parameters, (2) the application and network **conditions** under which "mechanism switching" reconfiguration is advantageous, and (3) the reconfiguration process overhead.

16/5/21 (Item 12 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

844238 ORDER NO: AAD84-10573
RANDOM MULTIPLE ACCESS METHODS IN MULTI-USER COMMUNICATION SYSTEMS (TREE ALGORITHMS)
Author: MERAKOS, LAZAROS FOTIS
Degree: PH.D.
Year: 1984
Corporate Source/Institution: STATE UNIVERSITY OF NEW YORK AT BUFFALO (0656)
Source: VOLUME 45/02-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 633. 220 PAGES
Descriptors: ENGINEERING, ELECTRONICS AND ELECTRICAL
Descriptor Codes: 0544

In a multi-user communication system a number of data transmitting users exchange information using a communication channel. Random access algorithms provide the means by which the capacity of the multiple access channel is shared by a large population of bursty users under distributed control. It is assumed that only one **message** at a time can be successfully transmitted over the channel. Users gain access into the channel on a contention basis, and utilize some form of broadcast feedback information to resolve their conflicts.

The first random access algorithm proposed is the "Aloha algorithm." The inherent instability of Aloha systems has stimulated research on Aloha-type retransmission control policies intended to stabilize these systems. We **introduce** criteria for measuring the efficiency of these policies. We use these measures to optimally select certain control parameters, to compare different first-time transmission policies, and to study the effect of reduced feedback information patterns and channel **errors** on the performance of the random access system.

" **Tree** algorithms" is a relatively new class of algorithms characterized by good throughput-delay **characteristics** and inherently stable operation. We propose and analyze a class of **Tree** -type algorithms with increased feedback. The proposed algorithms are stable within a substantially greater region of the input traffic at the expense of a small **message** overhead. The new algorithms are intended for systems whose long propagation delay makes the use of reservation schemes unattractive.

A serious drawback of some of the more efficient **Tree** algorithms is their sensitivity to **errors** in the feedback information. We analyze a robust algorithm with binary feedback, based on the assumption that users monitor the channel only when they have a **message** to send. We also **introduce** and analyze a new class of limited channel sensing algorithms for local area networks, where carrier sensing is available. These algorithms allow new **messages** to continuously enter into the system independently of the conflict resolution process already in progress. The "continuous **entry** " feature turns out to be instrumental for the robust properties of these schemes. We derive general sufficient **conditions** for stability, and we obtain lower bounds on the maximum stable throughput and upper bounds on the expected **message** delay. Our results show that these algorithms perform surprisingly well, guarantee long term stability, and combine limited channel sensing with robustness in the presence of feedback **errors** .

```
Set     Items   Description
S1    1271434   ENTRY? OR NODE? OR OBJECT? OR ENTRIES OR CHILD? OR PARENT?
            OR BRANCH?
S2    1502835   ATTRIBUTE? OR NAME? OR TIMESTAMP? OR FIELD? OR CHARACTERIS-
            TIC?
S3     429284   ERROR? OR INCORRECT? OR UNACCEPTABL? OR VERIF? OR WRONG? OR
             INVALID?
S4    1455415   MESSAG? OR ALERT? OR WARN? OR CONDITION? OR FLAG OR FLAGS
S5      74532   TREE OR TREES OR DIRECTORY OR DIRECTORIES OR BTREE OR RTREE
            OR TRIE OR TRIES OR DATA()(STRUCTURE?) OR DATASTRUCTURE?
S6    2734154   INSERT? OR ADD OR ADDS OR ADDED OR EMBED OR ADDING OR EMBE-
            DING OR INTRODUCE? OR INTRODUCING
S7          3   S1 AND S2 AND S3 AND S4 AND S5 AND S6
S8         24   S1 AND S2 AND S3 AND S5 AND S6
S9         15   S2 AND S3 AND S4 AND S5 AND S6
S10      9673   S6 AND S5
S11       320   S3 AND S10
S12        25   S11 AND IC=G06F-009
S13        36   S7:S9
S14        55   S12 OR S13
S15        44   S14 AND IC=G06F
S16        25   S15 NOT AD=20010802:20040802
S17        25   IDPAT (sorted in duplicate/non-duplicate order)
S18        25   IDPAT (primary/non-duplicate records only)
File 347:JAPIO Nov 1976-2005/Jan(Updated 050506)
        (c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200534
        (c) 2005  Thomson Derwent
```

18/5/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010928610 **Image available**
WPI Acc No: 1996-425561/199642
XRPX Acc No: N96-358223

Address translation method for computer - searching translation lookaside buffer and translation table held in memory and implemented as B- tree structure

Patent Assignee: FUJITSU LTD (FUIT); HAL COMPUTER SYSTEMS INC (HALC-N); HAL COMPUTERS SYSTEMS INC (HALC-N)
Inventor: CHANG C D; LIH Y; PENG L K
Number of Countries: 018 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9627834	A1	19960912	WO 96US2384	A	19960229	199642	B
US 5680566	A	19971021	US 95397809	A	19950303	199748	
EP 813713	A1	19971229	EP 96909505	A	19960229	199805	
			WO 96US2384	A	19960229		
JP 11501745	W	19990209	JP 96526888	A	19960229	199916	
			WO 96US2384	A	19960229		
US 5893931	A	19990413	US 95397809	A	19950303	199922	
			US 97783967	A	19970115		
EP 813713	B1	20030903	EP 96909505	A	19960229	200360	
			WO 96US2384	A	19960229		
DE 69629800	E	20031009	DE 629800	A	19960229	200374	
			EP 96909505	A	19960229		
			WO 96US2384	A	19960229		

Priority Applications (No Type Date): US 95397809 A 19950303; US 97783967 A 19970115
Cited Patents: US 4473878; US 5109355; US 5148533; US 5237671; US 5426750
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9627834	A1	E	50	G06F-012/10	
Designated States (National): JP					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
US 5680566	A		21	G06F-012/10	
EP 813713	A1	E		G06F-012/10	Based on patent WO 9627834
Designated States (Regional): DE FR GB					
JP 11501745	W		49	G06F-012/10	Based on patent WO 9627834
US 5893931	A			G06F-012/10	Cont of application US 95397809 Cont of patent US 5680566
EP 813713	B1	E		G06F-012/10	Based on patent WO 9627834
Designated States (Regional): DE FR GB					
DE 69629800	E			G06F-012/10	Based on patent EP 813713 Based on patent WO 9627834

Abstract (Basic): WO 9627834 A

The method for performing address translation in a computer system which supports virtual memory involves searching a translation lookaside buffer (101) (TLB) and possibly, a translation table (116) held in memory (106) and implemented as a B- **tree** structure. The TLB is initially searched for a translation for a specified input address (104). If exactly one valid **entry** of the TLB stores a translation for the specified input address, the output address (129) corresp to the specified input address is determined from the contents of that **entry** .

Otherwise, the translation table is searched for a translation for the specified input address. If two or more valid **entries** of the TLB store a translation for the specified input address, the **entries** are **invalidated** . A translation for the specified input address and possible one or more translations for other input addresses that are

stored together with the translation for the specified input addresses are taken from the translation table and **inserted** into the TLB.

USE - Preventing and recovering from situation where multiple translations in buffer corresp to same address.

Dwg.1b/10

Title Terms: ADDRESS; TRANSLATION; METHOD; COMPUTER; SEARCH; TRANSLATION; BUFFER; TRANSLATION; TABLE; HELD; MEMORY; IMPLEMENT; **TREE** ; STRUCTURE

Derwent Class: T01

International Patent Class (Main): **G06F-012/10**

International Patent Class (Additional): **G06F-017/30**

File Segment: EPI

18/5/15 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010402063 **Image available**
WPI Acc No: 1995-303376/199540
XRPX Acc No: N95-230464
Software generation system based memory error **detection** - inserting error **checking commands and additional information into parse** tree **associated with source code file being tested at read time to initiate and facilitate run-time** error **detection**
Patent Assignee: AMERICAN TELEPHONE & TELEGRAPH CO (AMTT); AT & T CORP (AMTT); LUCENT TECHNOLOGIES INC (LUCE)
Inventor: GOODNOW J E; KOWALSKI T J; ROWLAND J R
Number of Countries: 003 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 666535	A2	19950809	EP 95300460	A	19950126	199540	B
JP 7225703	A	19950822	JP 9539426	A	19950206	199542	
CA 2140084	A	19950805	CA 2140084	A	19950112	199543	
EP 666535	A3	19960228	EP 95300460	A	19950126	199622	
US 5590329	A	19961231	US 94192239	A	19940204	199707	

Priority Applications (No Type Date): US 94192239 A 19940204
Cited Patents: No-SR.Pub; 1.Jnl.Ref; US 5193180; WO 9300633
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 666535	A2	E	48	G06F-011/00	
JP 7225703	A		44	G06F-011/28	
US 5590329	A		38	G06F-011/08	
CA 2140084	A			G06F-011/30	
EP 666535	A3			G06F-011/00	

Abstract (Basic): EP 666535 A

The **error** detection method involves detecting the deferecning of an **invalid** pointer using a software program. Information including the last known contents and valid range are stored for each pointer. The information is updated each time the values are changed. A run-time pointer check is implemented each time a pointer deference is detected. The check involves locating the pointer information associated with the pointer and retrieving the actual contents of the pointer from the memory location where the pointer is stored.

The test is performed to determine whether the space pointed to by the actual pointer contents is within the valid range. The test is undertaken only if the actual contents of the pointer equals the last known contents to ensure that an **error** is not generated if the contents of the pointer was modified during execution of one of the library functions that was not detected by the system.

USE/ADVANTAGE - Testing and debugging software programs. Performs **error** detection whilst executing both interpreted source and compiled object code. Ensures that pointers are within acceptable bounds. Efficient operation.

Dwg.1/14

Title Terms: SOFTWARE; GENERATE; SYSTEM; BASED; MEMORY; **ERROR** ; DETECT; **INSERT** ; **ERROR** ; CHECK; COMMAND; **ADD** ; INFORMATION; PARSE; **TREE** ; ASSOCIATE; SOURCE; CODE; FILE; TEST; READ; TIME; INITIATE; FACILITATE; RUN; TIME; **ERROR** ; DETECT
Derwent Class: T01
International Patent Class (Main): **G06F-011/00** ; **G06F-011/08** ; **G06F-011/28** ; **G06F-011/30**
International Patent Class (Additional): **G06F-009/06** ; **G06F-012/14**
File Segment: EPI

18/5/22 (Item 22 from file: 347)
DIALOG(R)File 347:JAPIO

03776767 **Image available**
FILE MANAGING METHOD

PUB. NO.: 04-141867 [JP 4141867 A]
PUBLISHED: May 15, 1992 (19920515)
INVENTOR(s): HOSOYA HIDEKI
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-263774 [JP 90263774]
FILED: October 03, 1990 (19901003)
INTL CLASS: [5] G11B-020/12; **G06F-012/00** ; G11B-027/00
JAPIO CLASS: 42.5 (ELECTRONICS -- Equipment); 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1414, Vol. 16, No. 421, Pg. 71, September 04, 1992 (19920904)

ABSTRACT

PURPOSE: To enable effective management by recording additional data in the subsequent part of having read data when there is an **invalid** data part in the final recording information unit of a file at the time of recording additional data and **invalidating** a final recording unit area in a file whose **name** is the same and whose **flag** is more than a maximum value so as to control it at the time of reproduction.

CONSTITUTION: All final recording tracks in the file to be **added** are checked to be effective data or not. When a file capacity in a **directory** 301 for managing a file A(1) is not the integral multiple of the capacity of one track, **invalid** data comes to exist. In such a case, effective data 306 of the file A(1) to be **added** is read on a buffer memory 400 as data 401, and data 402 to be **added** is **added** in the subsequent part of it. At the time of reproduction, the file whose **name** is the same, whose **flag** is different and whose **flag** is more than the maximum value is managed with the final recording unit area as an **invalid** recording unit area. Thus, effective file management is enabled.

18/5/23 (Item 23 from file: 347)
DIALOG(R)File 347:JAPIO

03450737
ADDITION/CORRECTION METHOD FOR KNOWLEDGE OF EXPERT SYSTEM

PUB. NO.: 03-113637 [JP 3113637 A]
PUBLISHED: May 15, 1991 (19910515)
INVENTOR(s): HIRAMATSU TATSUO
APPLICANT(s): MEIDENSHA CORP [000610] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-253447 [JP 89253447]
FILED: September 28, 1989 (19890928)
INTL CLASS: [5] **G06F-009/44**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 1237, Vol. 15, No. 316, Pg. 71, August 13, 1991 (19910813)

ABSTRACT

PURPOSE: To reduce a compiling time by reading knowledge from a source file in the one processing unit of compiling, generating the arrangement of a data cell structural body and a syntax analysis **tree** by means of a knowledge expression language, interactively correcting the **tree** in a partial **tree** unit and generating object codes by terminating the check of all the source files.

CONSTITUTION: Knowledge **added** to the source files is read in the one processing unit of the compiling processing, the arrangement of the data cell structural body is generated, the arrangement of the data cell is performed the syntax analysis by the knowledge expression language, and the syntax analysis **tree** by the combination of the data cells is generated. When there is a grammatical **error** in the syntax analysis **tree** , a processing which interactively corrects the partial **tree** having the **error** is executed and the partial **tree** which is correction-processed is performed the syntax analysis by the knowledge expression language. Then, the grammatical **error** is checked again. When knowledge is **added** or corrected as to all the source files, the object codes are generated as to the files and they are written into an output file. Thus, the addition/correction of knowledge is facilitated.

```
Set     Items   Description
S1    1271434   ENTRY? OR NODE? OR OBJECT? OR ENTRIES OR CHILD? OR PARENT?
            OR BRANCH?
S2    1502835   ATTRIBUTE? OR NAME? OR TIMESTAMP? OR FIELD? OR CHARACTERIS-
            TIC?
S3    1312249   ERROR? OR INCORRECT? OR UNACCEPTABL? OR VERIF? OR WRONG? OR
            TEST? OR CHECK?
S4    1455415   MESSAG? OR ALERT? OR WARN? OR CONDITION? OR FLAG OR FLAGS
S5      61256   TREE OR TREES OR DIRECTORY OR DIRECTORIES OR BTREE OR RTREE
            OR TRIE
S6    2224183   INSERT? OR ADD OR EMBED OR ADDING OR EMBEDING OR INTRODUCE?
            OR INTRODUCING
S7          5   S1 AND S2 AND S3 AND S4 AND S5 AND S6
S8         29   S1 AND S2 AND S3 AND S5 AND S6
S9         22   S2 AND S3 AND S4 AND S5 AND S6
S10        46   S7:S9
S11        46   IDPAT (sorted in duplicate/non-duplicate order)
S12        46   IDPAT (primary/non-duplicate records only)
File 347:JAPIO Nov 1976-2005/Jan(Updated 050506)
         (c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200534
         (c) 2005  Thomson Derwent
```

12/5/17 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015386534 **Image available**
WPI Acc No: 2003-447478/200342
XRPX Acc No: N03-356827
Entry **addition method for** directory **operation, involves constructing** entry **comprising set of** attributes **not including location within** directory **information** tree **and destination location within** tree
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: BEHERA P; DORAI D; FU C; MAN H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030028752	A1	20030206	US 2001922190	A	20010802	200342	B

Priority Applications (No Type Date): US 2001922190 A 20010802
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030028752	A1		17	G06F-009/30	

Abstract (Basic): US 20030028752 A1
NOVELTY - A template comprising structural information of **directory** information **tree** , is read according to accessed template **tree** and a set of **attributes** not including a location within the **tree** , is received from an application program. An **entry** comprising the received **attributes** and a destination location within the **tree** , is constructed and added to the **tree** at the destination location.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for computer-readable medium storing **entry** addition program.
USE - For **adding entry** to **directory** information **tree** such as lightweight **directory** access protocol (LDAP) in computing device.
ADVANTAGE - Eases the task of maintaining **directory** service by eliminating the work to rewrite and **test** applications, when the structure of **directory** information **tree** is changed and the **errors** that occur when an application is rewritten.
DESCRIPTION OF DRAWING(S) - The figure shows the **directory** information **tree** .
pp; 17 DwgNo 1/9
Title Terms: ENTER; **ADD** ; METHOD; **DIRECTORY** ; OPERATE; CONSTRUCTION; ENTER; COMPRISE; SET; **ATTRIBUTE** ; LOCATE; **DIRECTORY** ; INFORMATION; **TREE** ; DESTINATION; LOCATE; **TREE**
Derwent Class: T01
International Patent Class (Main): G06F-009/30
File Segment: EPI

12/5/20 (Item 20 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014995620 **Image available**
WPI Acc No: 2003-056135/200305
Editor for constructing xml document
Patent Assignee: CHANGHAE SOFT SERVICE CO LTD (CHAN-N)
Inventor: LEE M N
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2002057709	A	20020712	KR 2001688	A	20010105	200305	B

Priority Applications (No Type Date): KR 2001688 A 20010105
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2002057709	A		1	G06F-017/24	

Abstract (Basic): KR 2002057709 A

NOVELTY - An XML(eXtensible Markup Language) document construction editor is provided to be applied to a design of various company documents, a DTD document, various public documents or attached documents in an electronic commerce and to support an easy edition function, a rapid search function, a document standardization, and a document effectiveness **check** function.

DETAILED DESCRIPTION - The editor comprises an XML engine, an element component, a table component, an XML **tree** view component, an XML editor component, an XSL(eXtensible Stylesheet Language) editor component, a DTD **tree** view component, a DTD editor component, an Explorer view component, and a designer component. The XML engine automatically performs a design process for constructing an XSL or XML document. The element component defines an **attribute** or a type for expressing data, **inserts** other element or a table within an element, expresses a picture according to a component type, automatically displays a DTD to an element after **checking** the DTD, automatically calculates a size and a position of a table or an element when the table or the element is included in a **child** of an element by an operation of a mouse, and copies an element. The table component performs a division, an synthesis, an inclusion or an **insertion** of a table element. The XML **tree** view component displays a **tree** when an XML document is constructed. The XML editor component displays data and a tag with different colors when displaying the text. The XSL editor component reads contents of an XSL document, and sets a color to a tag while displaying the contents. The DTD **tree** view component automatically draws an **attribute** and a type in a **tree** , and an icon relation diagram. The DTD editor component sets a color to the text for enhancing a readability.

pp; 1 DwgNo 1/10
Title Terms: EDIT; CONSTRUCTION; DOCUMENT
Derwent Class: T01
International Patent Class (Main): G06F-017/24
File Segment: EPI

2/5/28 (Item 28 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014275295 **Image available**
WPI Acc No: 2002-095997/200213
Method for managing t- tree index key at database in main memory
Patent Assignee: KOREA ELECTRONICS & TELECOM RES INST (KOEL-N)
Inventor: CHOI W; JUN G P; KIM S U; KIM W Y; LEE B S; LEE S S; YUM S M; JEON G P; KIM S W; YEOM S M
Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2001078492	A	20010821	KR 9956219	A	19991209	200213	B
KR 345445	B	20020726	KR 9956219	A	19991209	200308	

Priority Applications (No Type Date): KR 9956219 A 19991209
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2001078492	A		1	G06F-017/30	
KR 345445	B			G06F-017/30	Previous Publ. patent KR 2001078492

Abstract (Basic): KR 2001078492 A
NOVELTY - A T- **tree** index key management method is provided to effectively support a variable length key, a multiple **attribute** key and an overlapping key in a T- **tree** widely used in a main memory DBMS as an index structure.
DETAILED DESCRIPTION - The method comprises steps of **inserting** a newly allocated **node** in an **entry** if a root **node** is a null(101,102), replacing a current **node** with the root **node** if the root **node** is not a null(103), stopping a process if the current **node** is a null(104), comparing a key value of an **entry** with a minimum value of the current **node** if the current **node** is not a null(105), comparing the key value of the **entry** with a maximum value of the current **node** if the key value is larger, replacing the current **node** with a right side **child node** of the current **node** and then returning to the step 104 in the case that the key value is larger and the right side **child node** exists, **inserting** the **entry** in the current **node** and then stopping the process in the case that the right side **child node** does not exist and an **insertion** space exists at the current **node** , **inserting** the **entry** in the current **node** and then stopping the process in the case that the key value is not larger than the maximum value of the current **node** and an **insertion** space exists at the current **node** , deleting the minimum value at the current **node** and **inserting** the **entry** in the current **node** in the case that an **insertion** space does not exist, searching the lowest boundary **node** from the current **node** in the case that a left side **child node** exists at the current **node** , **inserting** a minimum of the current **node** in the case that a space exists at the boundary **node** , allocating a new **node** and **inserting** a minimum value in the space does not exist at the boundary **node** , **checking** if a left side **child node** exists at the current **node** in the case that the key value of the **entry** is smaller than a minimum value of the current **node** (118), replacing the current **node** with the left side **child node** in the case that the left side **child node** exists(119), **inserting** the **entry** and stopping the process in the case that the left side **child node** does not exist and a space exists at the current **node** (120,121), and allocating a new **node** , **inserting** the **entry** in the new **node** and stopping the process in the case that a space does not exist(120,122).
pp; 1 DwgNo 1/10
Title Terms: METHOD; MANAGE; **TREE** ; INDEX; KEY; DATABASE; MAIN; MEMORY
Derwent Class: T01
International Patent Class (Main): G06F-017/30
File Segment: EPI